AN-545A
Application Note

TELEVISION VIDEO IF AMPLIFIER USING INTEGRATED CIRCUITS

Prepared by
Applications Engineering

This applications note considers the requirements of the video IF amplifier section of a television receiver, and gives working circuit schematics using integrated circuits which have been specifically designed for consumer oriented products. The integrated circuits used are the MC1350, MC1352, and the MC1330.

MOTOROLA *Semiconductor Products Inc.*

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INTRODUCTION

The very stringent requirements of the television video IF amplifier can now be met using integrated circuits while giving a substantial increase in performance and cost saving over conventional discrete components. Circuit techniques that would not have been technically or economically possible with discrete components, can now be utilized with integrated circuits.

Figure 1 indicates the signal levels and degree of automatic gain control (AGC) required if a television receiver is to function correctly throughout the range of input signal conditions commonly encountered. In some locations, all TV channels may provide high level signals, or conversely, all channels appear as low level signals. However, in most practical situations, each channel has its own amplitude. Some signals are nearly lost in noise, while others approach overload strength. This range of field intensity at the antenna requires AGC compensation in the television receiver over a dynamic range greater than 90 dB. Some of this control can be accomplished in the tuner, since a good solid-state TV tuner has an AGC reduction capability usually greater than 36 dB. The difference of at least 60 dB must be provided by the video IF amplifier.

The detected video output level will depend on the video amplifier and picture tube drive requirements. In the extreme case of a single stage, tube video amplifier, as used in inexpensive monochrome receivers, the level could be as high as 6 V. But in most hybrid and all solid-state receivers a one to two volt composite video and sync signal is sufficient. Figure 2 shows a block diagram using two integrated circuits, which gives the required IF gain, more than adequate AGC gain reduction, and a detected composite video output signal level of up to six volts, if required.

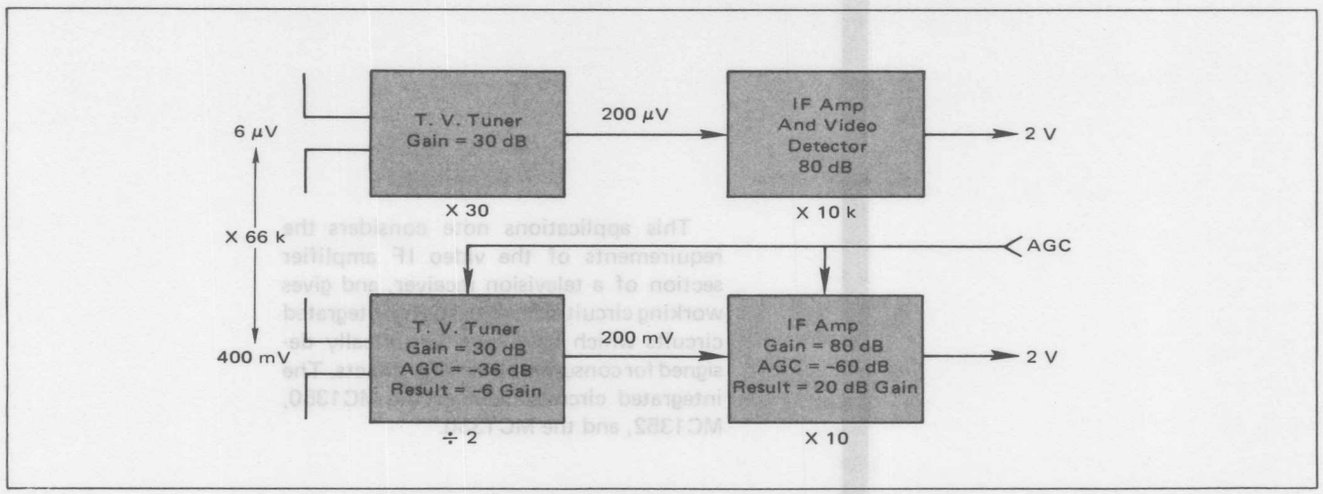


FIGURE 1 – Signal Levels and AGC Reduction Requirements for a Typical Television Receiver

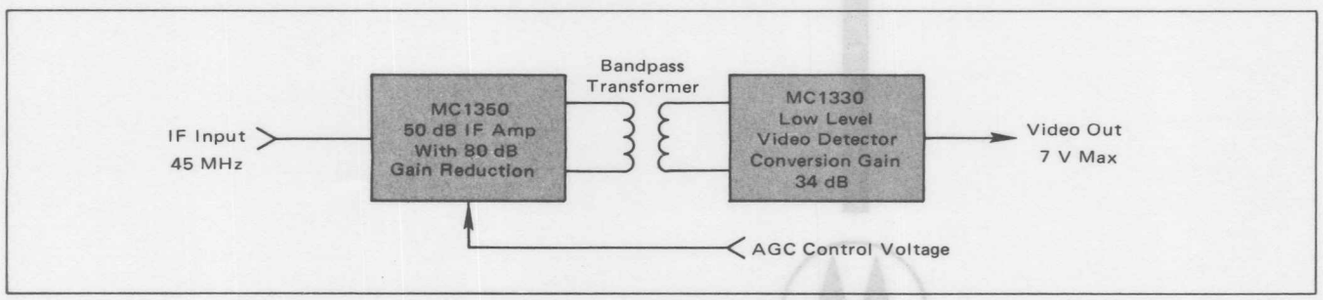


FIGURE 2 – Block Diagram of an IC Television Video IF Amplifier

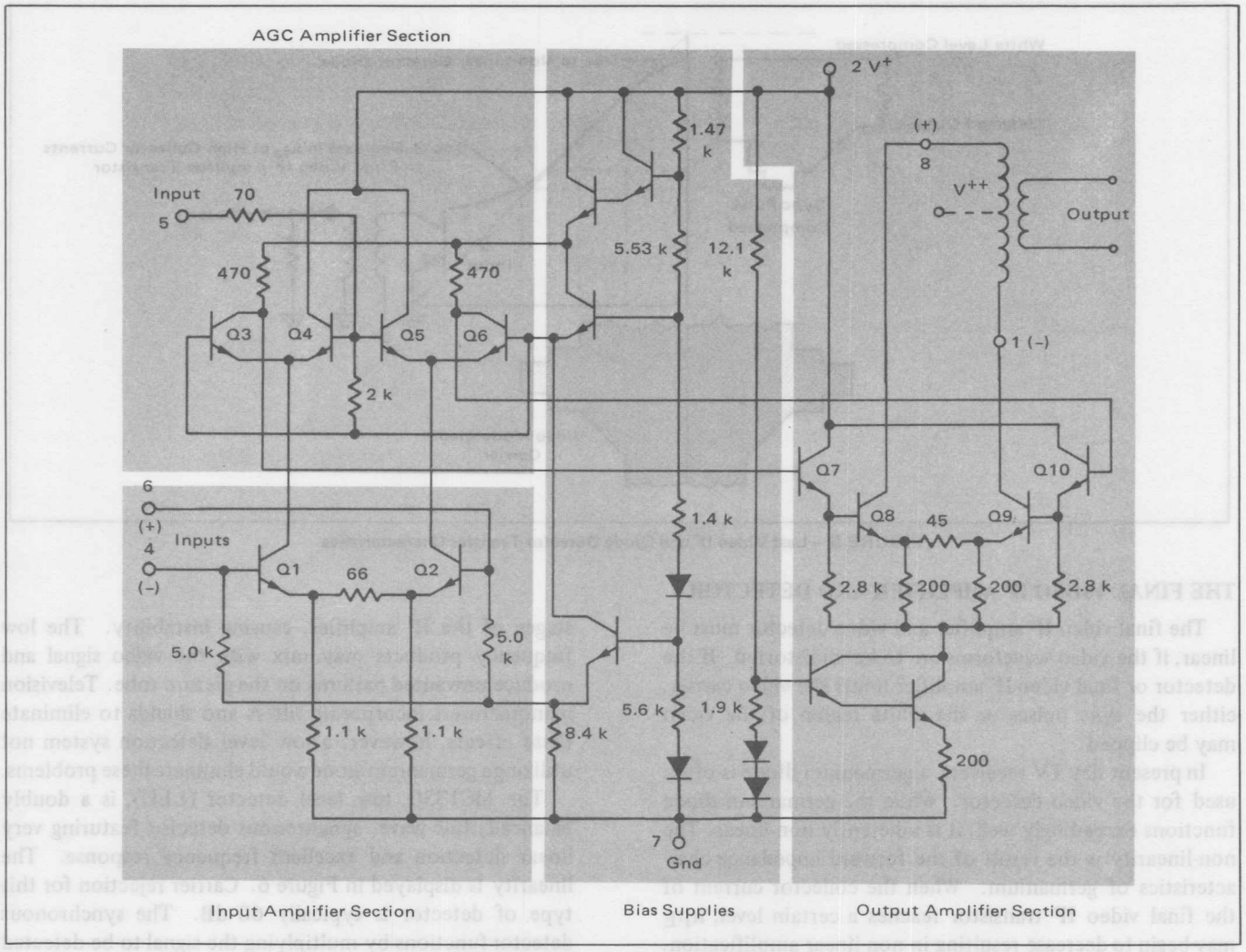


FIGURE 3 – Circuit Schematic

CIRCUIT DESCRIPTION – MC1350

Figure 3 is a schematic diagram of the MC1350, video IF amplifier. Q1, Q2, Q3, and Q6 form a differential cascade amplifier. When Q4 and Q5 are not conducting, the amplifier is at maximum gain. With a positive AGC bias voltage applied to the bases of Q4 and Q5, they will conduct and shunt away the signal current of Q3 and Q6. This will attenuate the gain of the amplifier, although the collector currents of Q1 and Q2 will remain constant preventing a large input impedance change. The output amplifiers, Q7, Q8, Q9, and Q10, are supplied from an active current source that maintains a constant quiescent bias keeping the output admittance nearly constant over the AGC range. The differential output is taken from the collectors of Q8 and Q9, however single-ended output may be taken from either collector, provided the unused collector is connected to the positive supply (V^+). Operation in this latter mode reduces the circuit gain. Either differential or single-ended inputs may be applied to Q1 and Q2. For single-ended input, there will be no loss in gain provided the unused input is grounded through a capacitor.

Figure 4 is a graph of the AGC gain reduction characteristics versus the voltage applied to Pin 5, through a 5 kΩ resistor.

In later paragraphs a more complex, keyed or gated AGC system will be discussed.

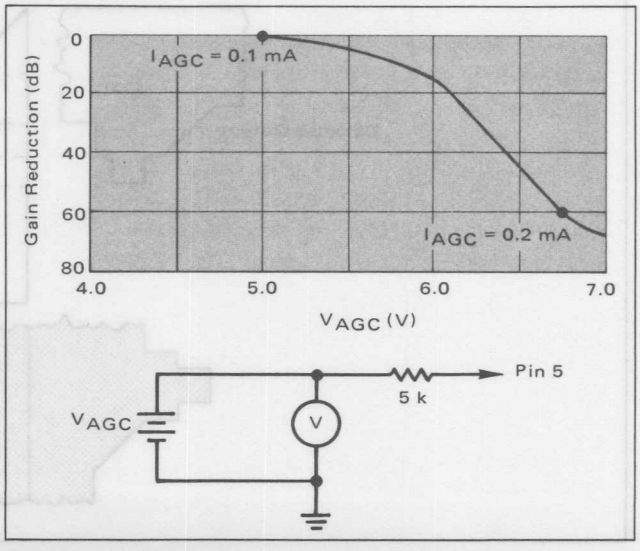


FIGURE 4 – Typical Gain Reduction

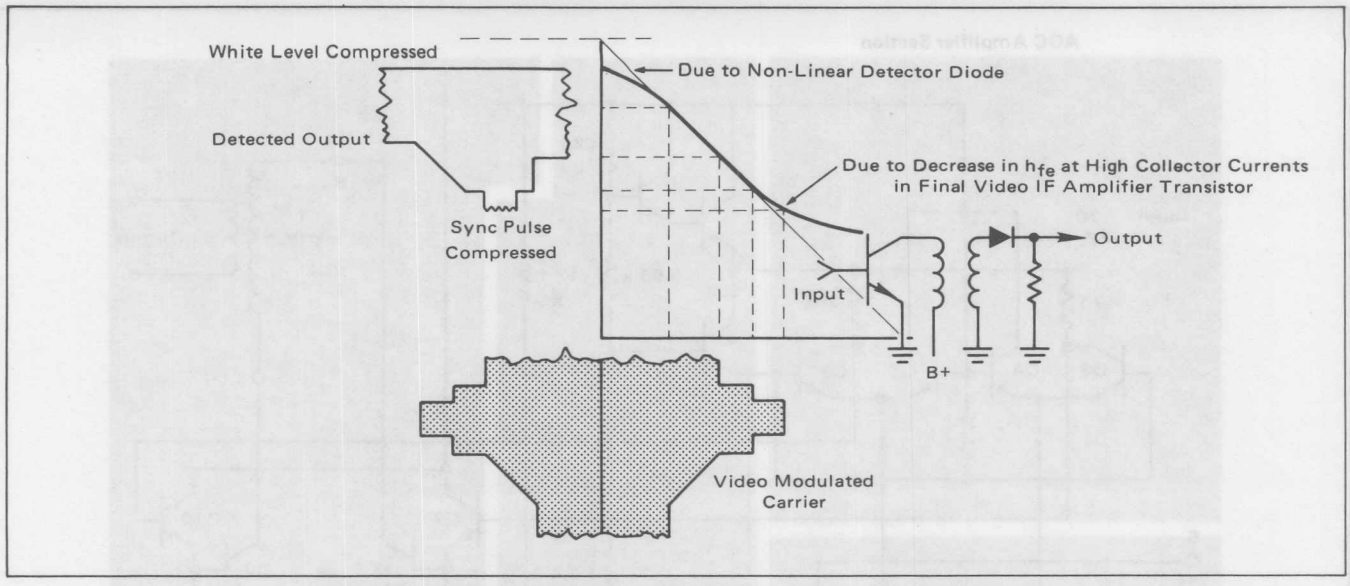


FIGURE 5 – Last Video IF and Diode Detector Transfer Characteristics

THE FINAL VIDEO IF AMPLIFIER AND DETECTOR

The final video IF amplifier and video detector must be linear, if the video waveforms are to be undistorted. If the detector or final video IF amplifier limits the video carrier, either the sync pulses or the white region of the video may be clipped.

In present day TV receivers, a germanium diode is often used for the video detector. While the germanium diode functions exceedingly well, it is inherently non-linear. The non-linearity is the result of the forward impedance characteristics of germanium. When the collector current of the final video IF transistor reaches a certain level, h_{FE} may begin to decrease resulting in non-linear amplification. Both of these effects are illustrated in Figure 5. These non-linearities generate unwanted sum and difference frequencies ("tweets"). The high frequency tweets may radiate into either the receiver antenna input, or into the low level stages of the IF amplifier, causing instability. The low frequency products may mix with the video signal and produce unwanted patterns on the picture tube. Television manufacturers incorporate filters and shields to eliminate these effects, however, a low level detection system not utilizing a germanium diode would eliminate these problems.

The MC1330, low level detector (LLD), is a doubly balanced, full wave, synchronous detector featuring very linear detection and excellent frequency response. The linearity is displayed in Figure 6. Carrier rejection for this type of detector is typically 60 dB. The synchronous detector functions by multiplying the signal to be detected by the same signal which has been amplified and limited. (See Figure 7.) Further information on low level detectors may be obtained in Motorola Application Notes AN-489 and AN-490.

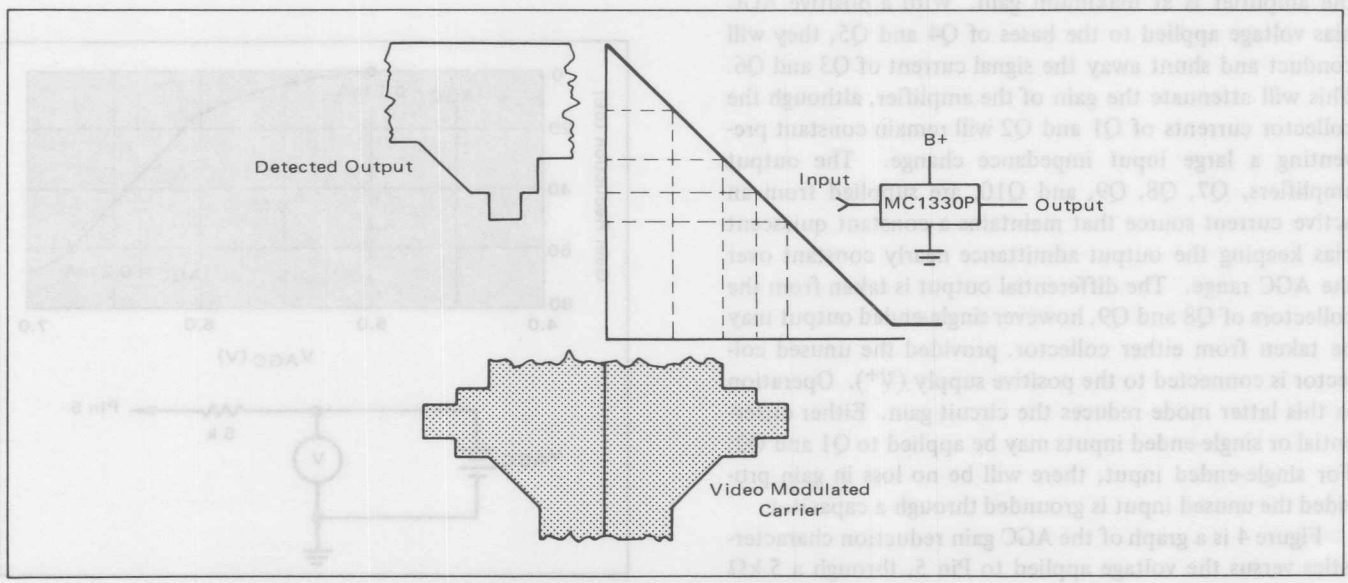


FIGURE 6 – MC1330P Linear Transfer Characteristics

CIRCUIT DESCRIPTION – MC1330

Figure 8 is a simplified circuit diagram of the MC1330. Q7 is a constant current source, Q1 and Q2 form a differential amplifier, while Q3, Q4, Q5, and Q6 are carrier operated switches. When positive half cycles of the amplitude modulated carrier appear at the base of Q1, it begins to conduct. The in-phase, clipped carrier signal will turn on Q3 causing current flow through R1 to increase. No current will flow through Q4, because it is switched off.

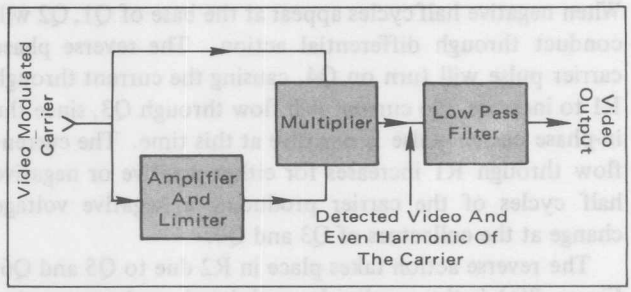


FIGURE 7 – Block Diagram of Low Level Detector

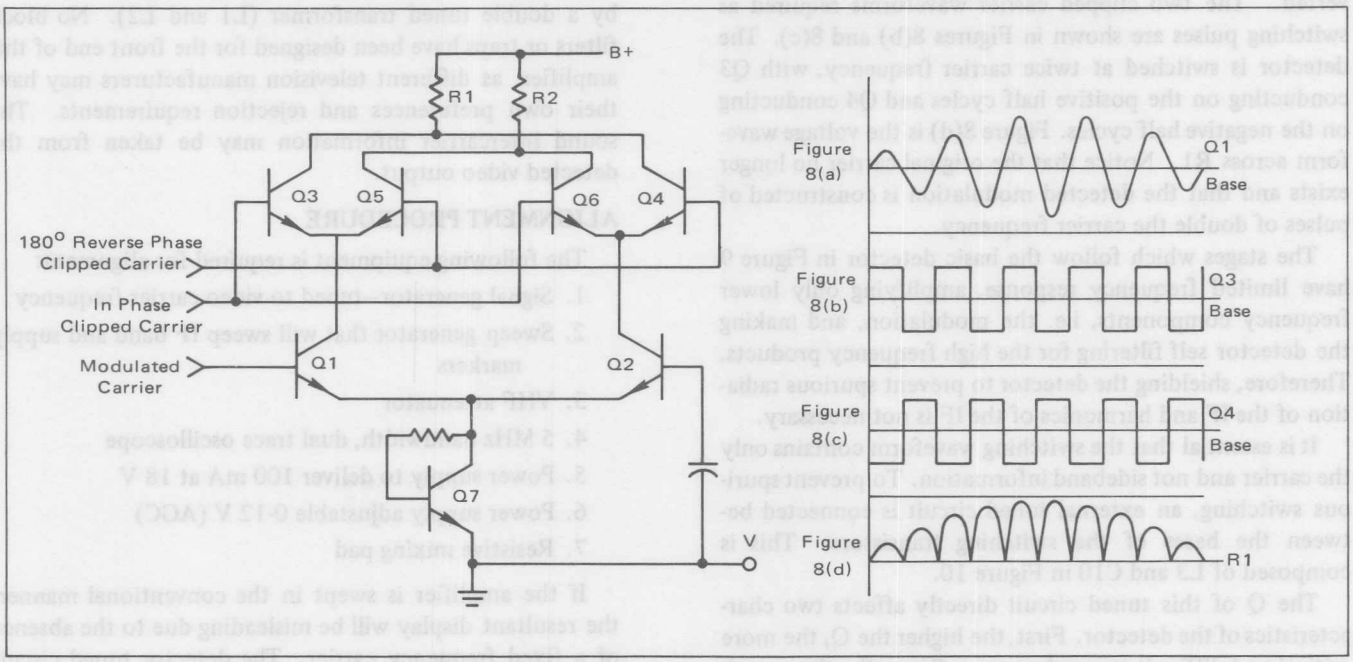


FIGURE 8 – Simplified Schematic of MC1330 and Waveforms

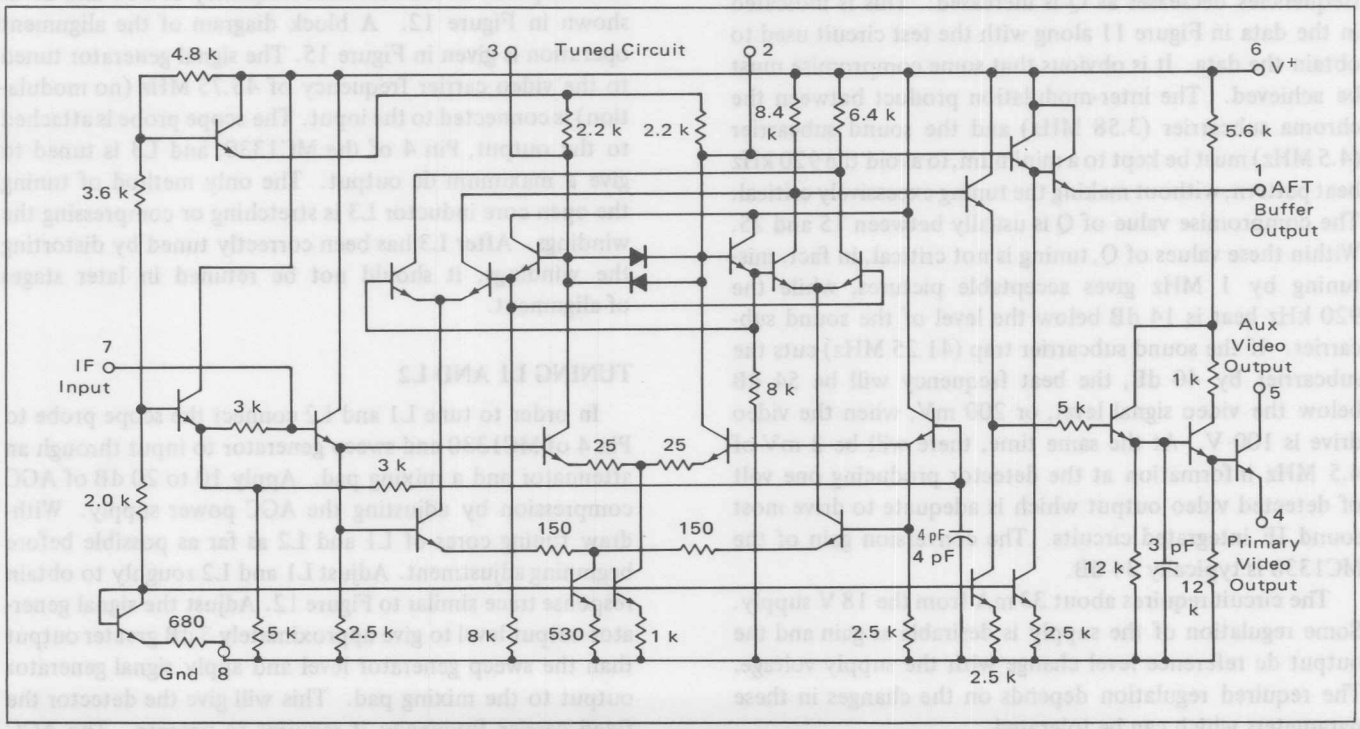


FIGURE 9 – Circuit Schematic

When negative half cycles appear at the base of Q1, Q2 will conduct through differential action. The reverse phase carrier pulse will turn on Q4, causing the current through R1 to increase. No current will flow through Q3, since the in-phase carrier pulse is negative at this time. The current flow through R1 increases for either positive or negative half cycles of the carrier producing a negative voltage change at the collectors of Q3 and Q4.

The reverse action takes place in R2 due to Q5 and Q6. Figure 8(a) is the amplitude modulated carrier appearing at the base of Q1. Q2 would see the same waveform inverted. The two clipped carrier waveforms required as switching pulses are shown in Figures 8(b) and 8(c). The detector is switched at twice carrier frequency, with Q3 conducting on the positive half cycles and Q4 conducting on the negative half cycles. Figure 8(d) is the voltage waveform across R1. Notice that the original carrier no longer exists and that the detected modulation is constructed of pulses of double the carrier frequency.

The stages which follow the basic detector in Figure 9 have limited frequency response, amplifying only lower frequency components, i.e. the modulation, and making the detector self filtering for the high frequency products. Therefore, shielding the detector to prevent spurious radiation of the IF and harmonics of the IF is not necessary.

It is essential that the switching waveform contains only the carrier and not sideband information. To prevent spurious switching, an external tuned circuit is connected between the bases of the switching transistors. This is composed of L3 and C10 in Figure 10.

The Q of this tuned circuit directly affects two characteristics of the detector. First, the higher the Q, the more critical and difficult tuning becomes. Secondly, the magnitude of the sum and difference products of two modulating frequencies decreases as Q is increased. This is indicated in the data in Figure 11 along with the test circuit used to obtain the data. It is obvious that some compromise must be achieved. The inter-modulation product between the chroma subcarrier (3.58 MHz) and the sound subcarrier (4.5 MHz) must be kept to a minimum, to avoid the 920 kHz beat pattern, without making the tuning excessively critical. The compromise value of Q is usually between 15 and 25. Within these values of Q, tuning is not critical, in fact, mistuning by 1 MHz gives acceptable pictures, while the 920 kHz beat is 14 dB below the level of the sound subcarrier. If the sound subcarrier trap (41.25 MHz) cuts the subcarrier by 40 dB, the beat frequency will be 54 dB below the video signal level, or 200 mV, when the video drive is 100 V. At the same time, there will be 2 mV of 4.5 MHz information at the detector producing one volt of detected video output which is adequate to drive most sound IF integrated circuits. The conversion gain of the MC1330 is typically 34 dB.

The circuit requires about 33 mA from the 18 V supply. Some regulation of the supply is desirable as gain and the output dc reference level change with the supply voltage. The required regulation depends on the changes in these parameters which can be tolerated.

A PRACTICAL TELEVISION IF AMPLIFIER AND DETECTOR

Figure 10 shows a complete practical circuit for an integrated circuit, video IF amplifier. This circuit employs the two integrated circuits previously discussed. This circuit has a typical voltage gain of 84 dB and a typical AGC range of 80 dB. It gives very small changes in bandpass shape, usually less than 1 dB tilt for 60 dB compression. There are no shielded sections. The detector uses a single tuned circuit (L3 and C10).

Coupling between the two integrated circuits is achieved by a double tuned transformer (L1 and L2). No block filters or traps have been designed for the front end of this amplifier, as different television manufacturers may have their own preferences and rejection requirements. The sound intercarrier information may be taken from the detected video output.

ALIGNMENT PROCEDURE

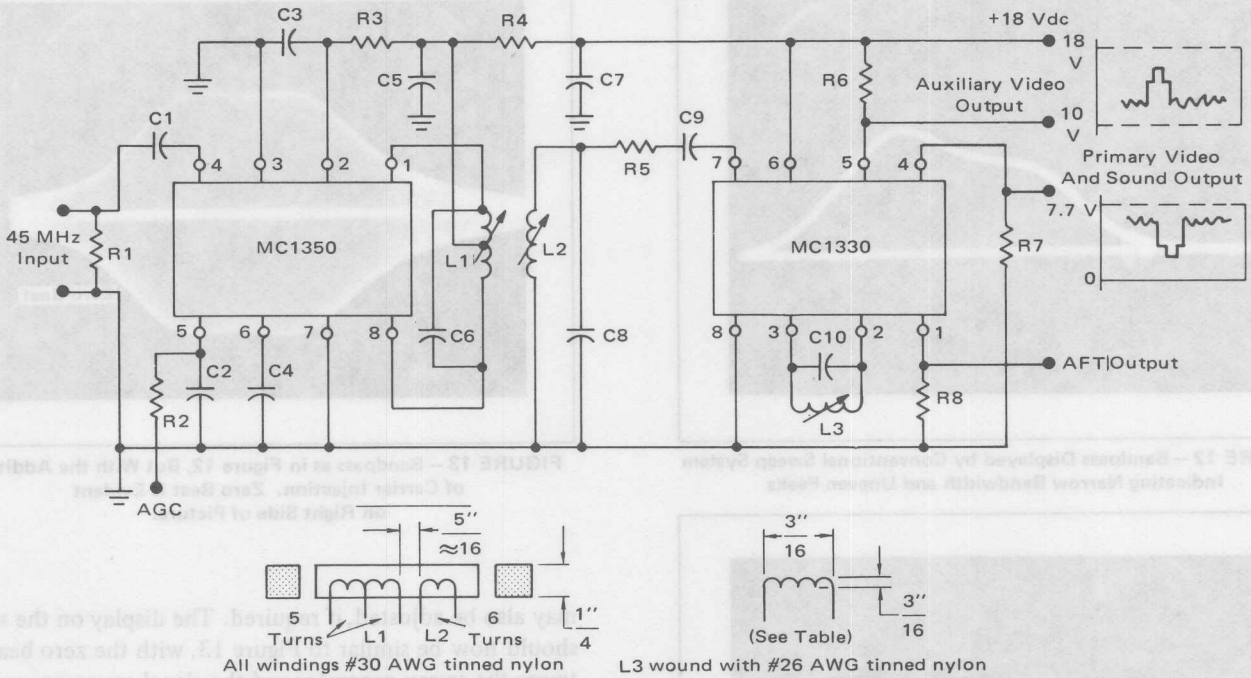
The following equipment is required for alignment:

1. Signal generator—tuned to video carrier frequency
2. Sweep generator that will sweep IF band and supply markers
3. VHF attenuator
4. 5 MHz bandwidth, dual trace oscilloscope
5. Power supply to deliver 100 mA at 18 V
6. Power supply adjustable 0-12 V (AGC)
7. Resistive mixing pad

If the amplifier is swept in the conventional manner, the resultant display will be misleading due to the absence of a fixed frequency carrier. The detector tuned circuit will follow the sweep generator and indicate a high amplitude response at the resonant frequency of C10 and L3 as shown in Figure 12. A block diagram of the alignment operation is given in Figure 15. The signal generator tuned to the video carrier frequency of 45.75 MHz (no modulation) is connected to the input. The scope probe is attached to the output, Pin 4 of the MC1330, and L3 is tuned to give a maximum dc output. The only method of tuning the open core inductor L3 is stretching or compressing the windings. After L3 has been correctly tuned by distorting the windings, it should not be retuned in later stages of alignment.

TUNING L1 AND L2

In order to tune L1 and L2 connect the scope probe to Pin 4 of MC1330 and sweep generator to input through an attenuator and a mixing pad. Apply 10 to 20 dB of AGC compression by adjusting the AGC power supply. Withdraw tuning cores of L1 and L2 as far as possible before beginning adjustment. Adjust L1 and L2 roughly to obtain response trace similar to Figure 12. Adjust the signal generator output level to give approximately 3 dB greater output than the sweep generator level and apply signal generator output to the mixing pad. This will give the detector the fixed carrier frequency it requires to operate. The AGC



All windings #30 AWG tinned nylon acetate wire tuned with high permiability slugs. Coil Craft #4786 differential transformer.

L3 wound with #26 AWG tinned nylon acetate wire tuned by distorting winding.

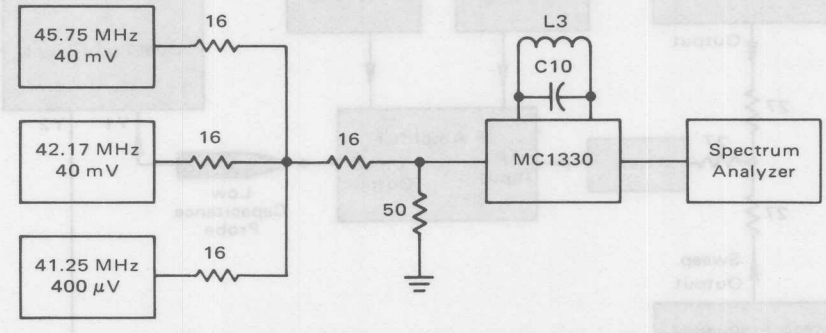
C1 = 0.001 μF
C2 = 0.002 μF
C3 = 0.002 μF
C4 = 0.002 μF
C5 = 0.002 μF
C6 = See Table
C7 = 0.1 μF
C8 = See Table
C9 = 68 pF
C10 = See Table
R1 = 50 Ω
R2 = 5 k
R3 = 470 Ω
R4 = 220 Ω
R5 = 22 Ω
R6 = 3.3 kΩ
R7 = 3.9 kΩ
R8 = 3.9 kΩ
All Resistors 1/4-W ±10%

All Caps Marked μF Ceramic HiK
All Caps Marked pF Silver Mica 5%

Table of Component Values

Component	36 MHz	45 MHz	58 MHz
C6	24 pF	15 pF	10 pF
C8	18 pF	12 pF	10 pF
C10	33 pF	33 pF	18 pF
L3	12 Turns	10 Turns	10 Turns

FIGURE 10 – Typical MC1350 Video IF Amplifier and MC1330 Low-Level Video Detector Circuit



Intermodulation Products as Measured in Above Circuit

Loaded Q	920 kHz	2.68 MHz	3.58 MHz	4.5 MHz	6.3 MHz	7.16 MHz	84 MHz	45.75 MHz	91.5 MHz
3	-45 dB	-60 dB	0 dB	-41 dB	-65 dB	-14 dB	-50 dB	-59 dB	-52 dB
15	-54 dB	-60 dB	0 dB	-41 dB	-65 dB	-15 dB	-50 dB	-59 dB	-52 dB
20	-56 dB	-62 dB	0 dB	-41 dB	-65 dB	-17 dB	-51 dB	-59 dB	-52 dB
50	-60 dB	-68 dB	0 dB	-41 dB	–	-21 dB	-55 dB	-59 dB	-52 dB

FIGURE 11 – Test Circuit for Intermodulation Products

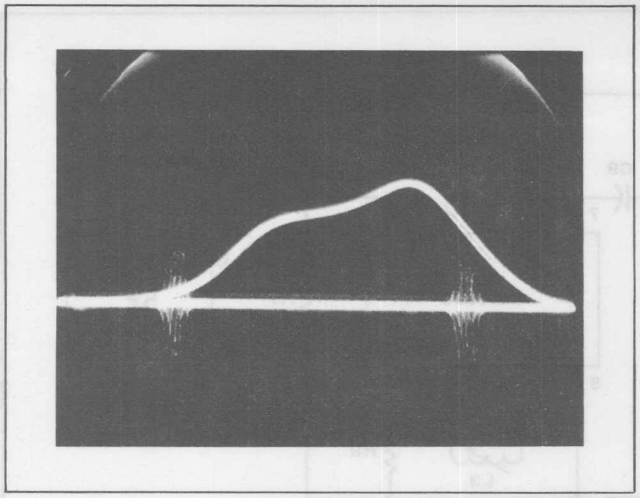


FIGURE 12 – Bandpass Displayed by Conventional Sweep System Indicating Narrow Bandwidth and Uneven Peaks

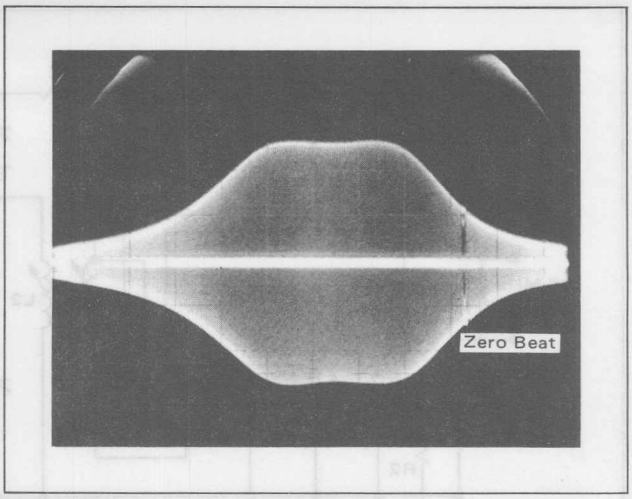


FIGURE 13 – Bandpass as in Figure 12, But With the Addition of Carrier Injection. Zero Beat is Evident on Right Side of Picture.

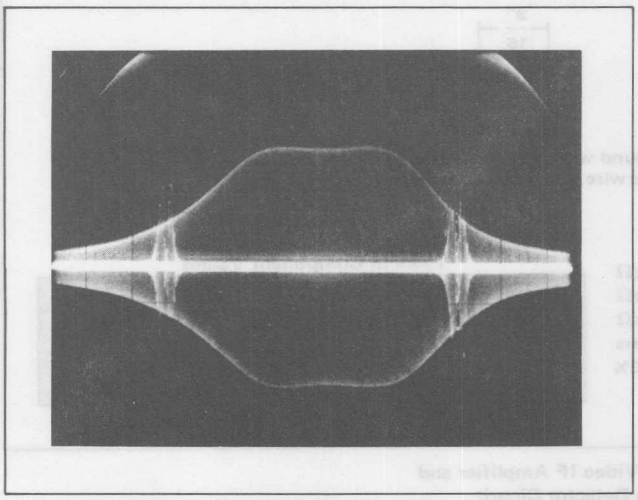


FIGURE 14 – Bandpass as in Figure 12, But With the Addition of Marker Frequencies

may also be adjusted, if required. The display on the scope should now be similar to Figure 13, with the zero beat between the sweep generator and the signal generator appearing within the modulation envelope. Adjust the second trace of the scope to display the marker frequencies, and adjust L1 and L2 to give bandpass shape as required. (See Figure 14.) L1 and L2 should be tuned to the first peak as the cores are turned into the windings to avoid over coupling.

A full-sized (1:1) printed circuit board layout is given in Figure 16. The components are identified as in the schematic diagram.

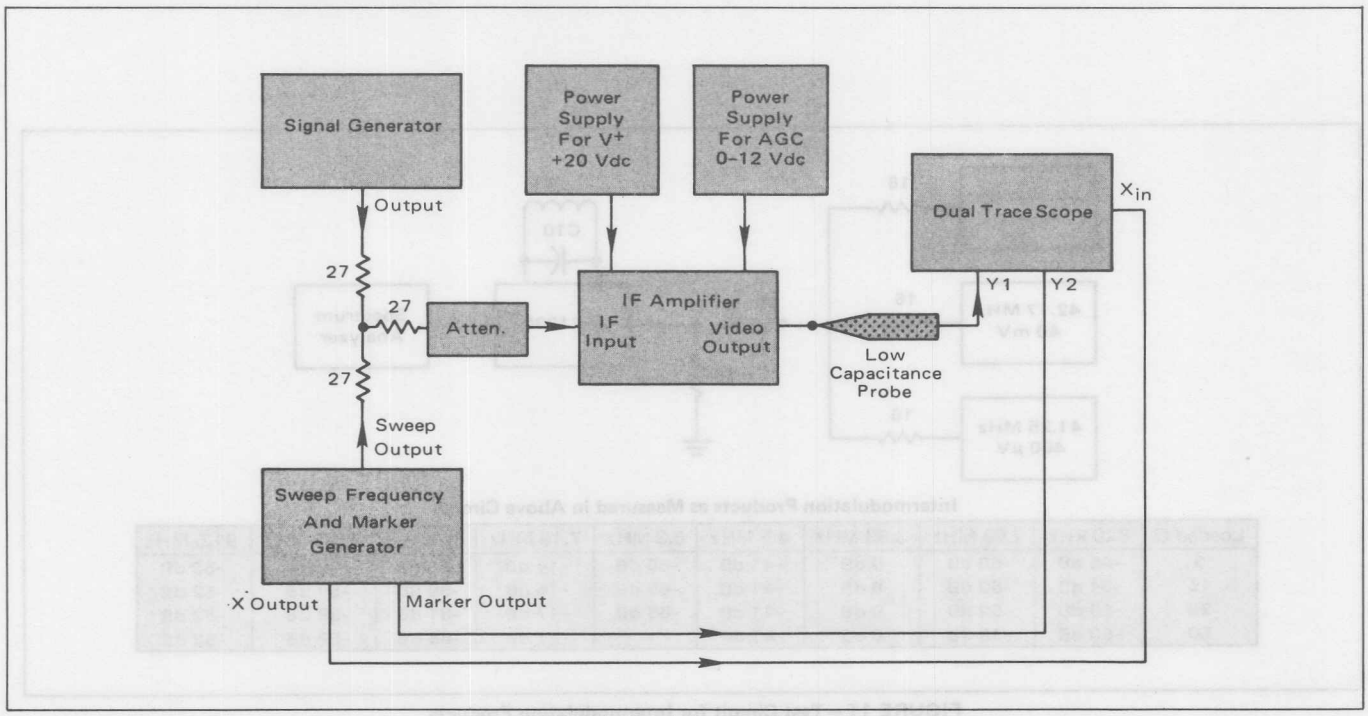


FIGURE 15 – Alignment Schematic

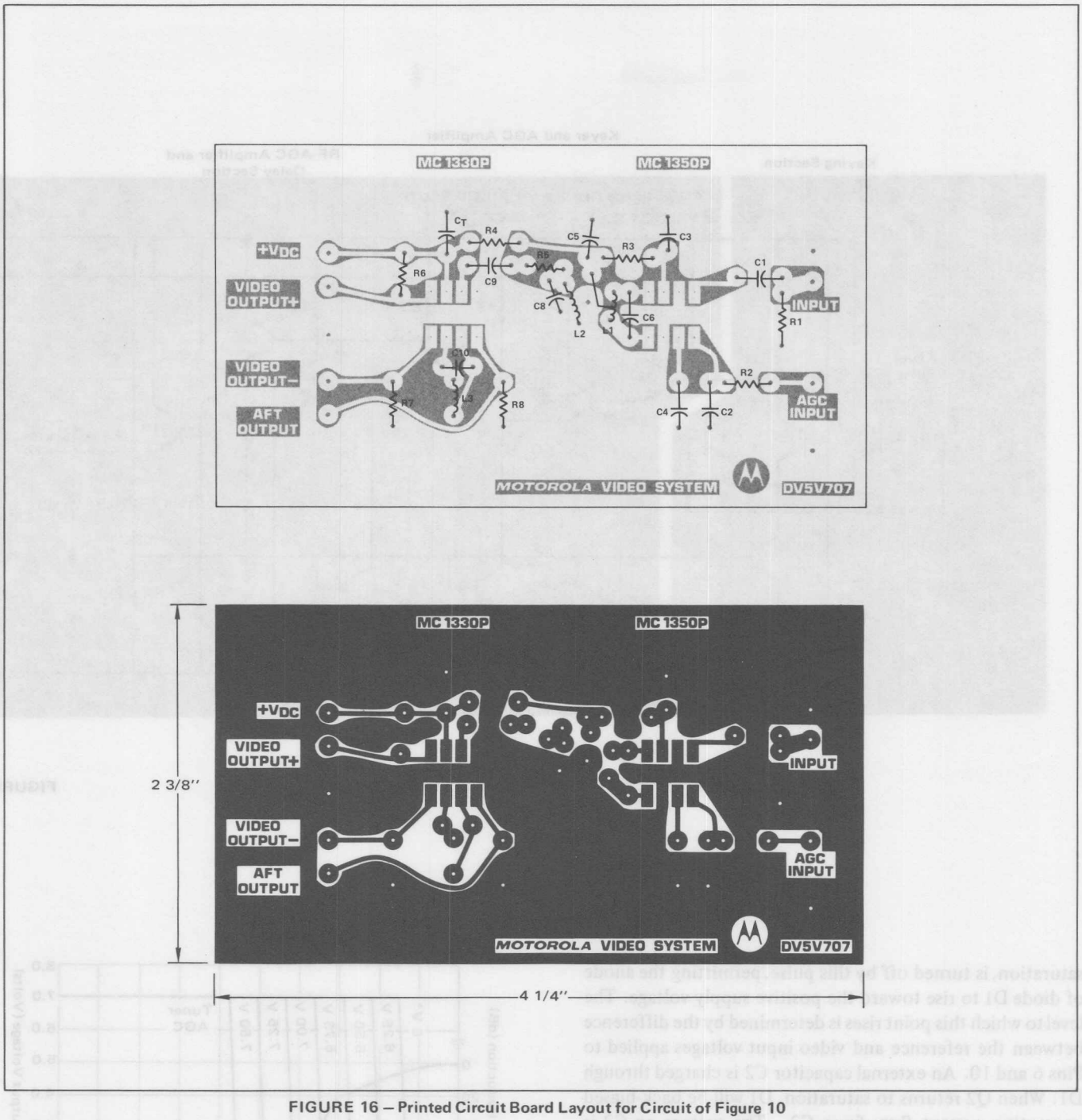


FIGURE 16 – Printed Circuit Board Layout for Circuit of Figure 10

AUTOMATIC GAIN CONTROL – MC1352

The IF amplifier previously described will require AGC from an external source. However, there is another integrated circuit for IF amplifier applications which replaces the MC1350 and has built-in keyed AGC. The MC1352 has a positive-going AGC output. The schematic is given in Figure 17. A gating pulse, a reference level, and the composite video signal to be controlled are required for correct operation of this AGC system. If positive-going video (with negative sync) is available, apply it to Pin 6 and apply the reference voltage to Pin 10. However, if negative-going video (with positive sync) is used, apply it to Pin 10 and the reference voltage to Pin 6. The magnitude of the reference voltage determines the AGC threshold.

CIRCUIT DESCRIPTION – MC1352

A negative keying pulse of eight volts amplitude and timed to each sync pulse is taken from the horizontal time base. This pulse is applied to Pin 5. Q2, normally in

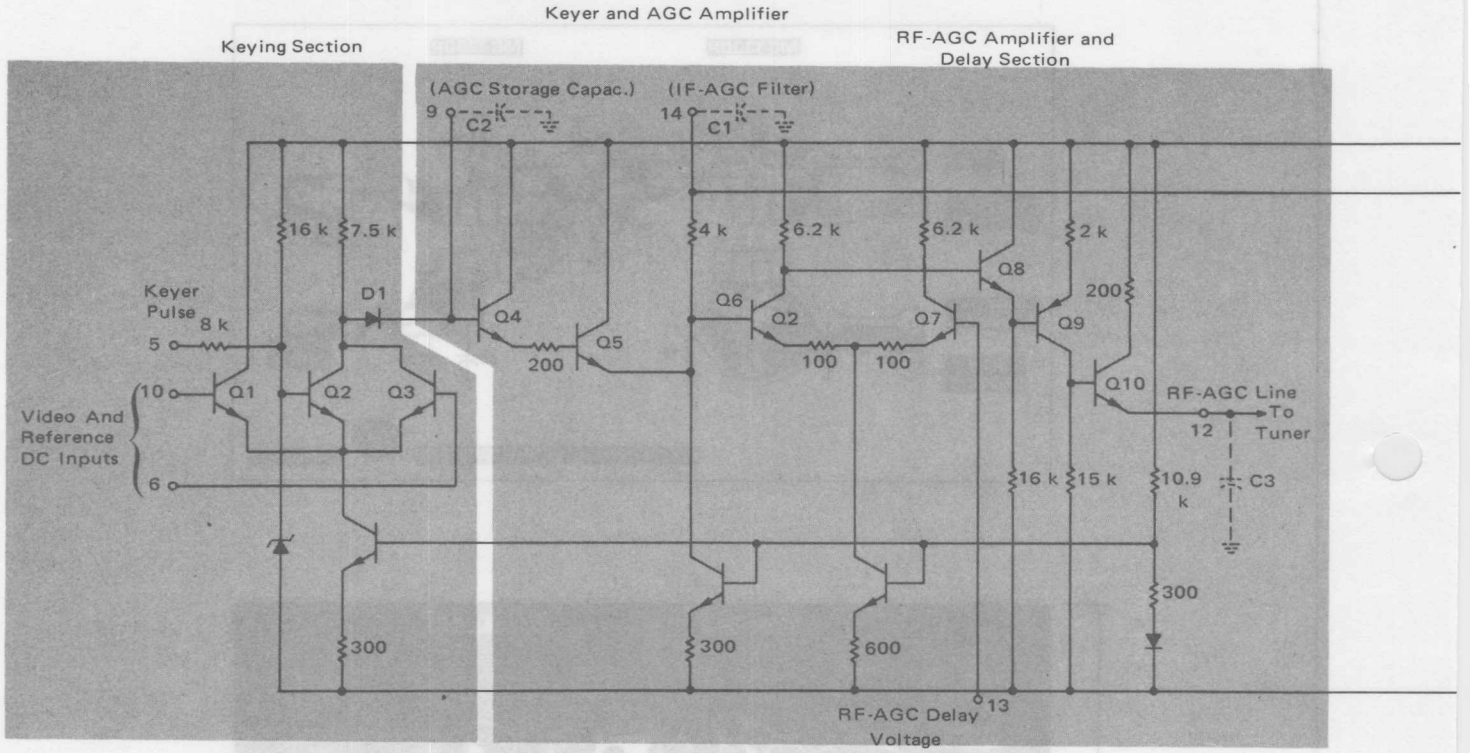


FIGURE 17 – Circuit

saturation, is turned off by this pulse, permitting the anode of diode D1 to rise toward the positive supply voltage. The level to which this point rises is determined by the difference between the reference and video input voltages applied to Pins 6 and 10. An external capacitor C2 is charged through D1. When Q2 returns to saturation, D1 will be back-biased preventing current flow from C2. The voltage on C2 is amplified by Q4 and Q5 and filtered by R1 and C1. The filtered voltage is supplied to the bases of Q12 and Q14 controlling the IF gain as described in the previous section on the MC1350. Q6 and Q7 form a differential amplifier. The amplified voltage from the capacitor is also applied to the base of Q6, while a delay voltage is applied to the base of Q7 through Pin 13. The delay voltage is used to determine the AGC threshold of the tuner. The output of the differential amplifier is taken from the collector of Q6 giving positive AGC action. Q8, Q9, and Q10 amplify the difference voltage (delayed AGC voltage) permitting gain control in the tuner. The full RF amplifier AGC compression is obtained with a much smaller change in video input voltage than required for full AGC ccompression in the IF amplifier. Figure 18 displays the AGC characteristics of the MC1352.

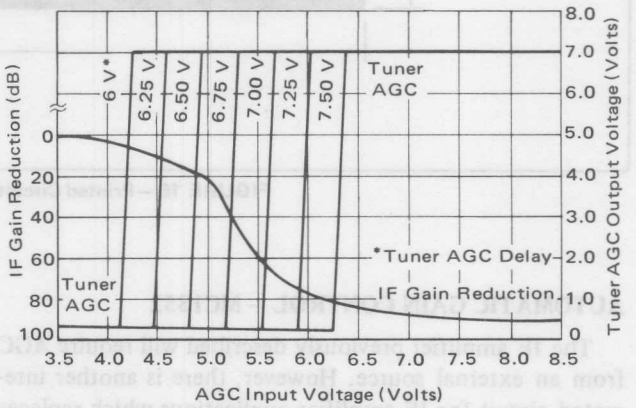
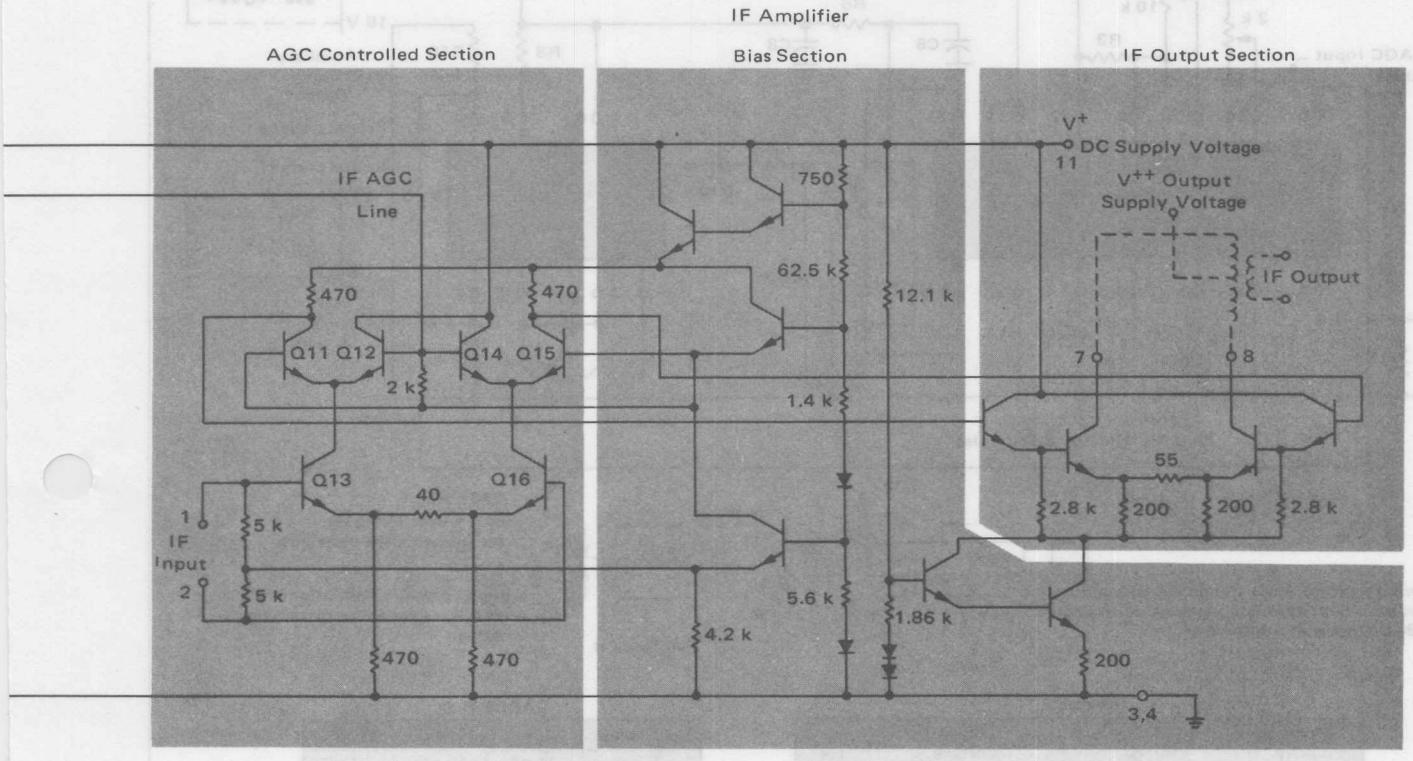


FIGURE 18 – MC1352 AGC Characteristics



iagram of MC1352

ADJUSTMENT OF RF AMPLIFIER BIAS

Figure 20 is a schematic diagram of a video IF amplifier for use at 45 MHz using an MC1330 low level detector and a MC1352. If the RF amplifier transistor in the tuner is an NPN device, a MC1352 is used. To set the maximum gain pre-bias on a forward AGC NPN transistor, a fixed resistor R_{pb} must be selected. This forms a voltage divider with the 6.8 kΩ resistor (R3). In the maximum gain condition, the voltage on Pin 12 would be zero volts without the voltage divider. To pre-bias a forward AGC PNP transistor, R_{pb} is set at 6.8 kΩ and R3 is selected for proper pre-bias. To obtain maximum gain without AGC control, for alignment purposes connect a 22 kΩ resistor between Pins 9 and 11 of the MC1352. Connecting a 200 kΩ variable resistor between Pin 14 and ground and also the 22 kΩ resistor between Pins 9 and 11 provides a method of obtaining any particular gain desired. The alignment procedure for Figure 20 is the same as described earlier for the MC1350. Additional information on the MC1352 can be obtained from the data sheet.

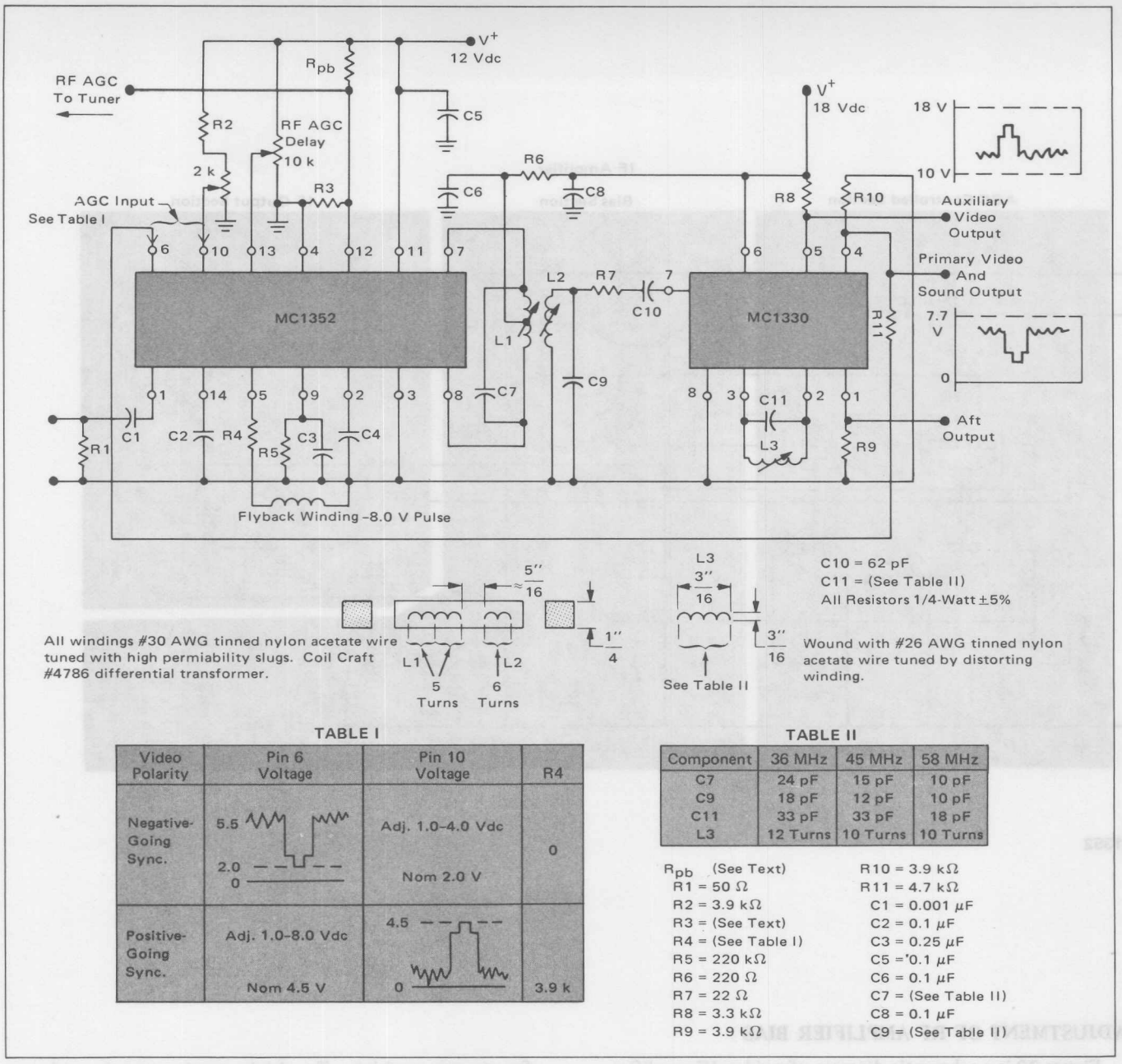


TABLE I

Video Polarity	Pin 6 Voltage	Pin 10 Voltage	R4
Negative-Going Sync.	5.5 / 2.0 / 0	Adj. 1.0-4.0 Vdc Nom 2.0 V	0
Positive-Going Sync.	Adj. 1.0-8.0 Vdc Nom 4.5 V	4.5 / 0	3.9 k

TABLE II

Component	36 MHz	45 MHz	58 MHz
C7	24 pF	15 pF	10 pF
C9	18 pF	12 pF	10 pF
C11	33 pF	33 pF	18 pF
L3	12 Turns	10 Turns	10 Turns

R_{pb} (See Text)
R1 = 50 Ω
R2 = 3.9 kΩ
R3 = (See Text)
R4 = (See Table I)
R5 = 220 kΩ
R6 = 220 Ω
R7 = 22 Ω
R8 = 3.3 kΩ
R9 = 3.9 kΩ
R10 = 3.9 kΩ
R11 = 4.7 kΩ
C1 = 0.001 μF
C2 = 0.1 μF
C3 = 0.25 μF
C5 = 0.1 μF
C6 = 0.1 μF
C7 = (See Table II)
C8 = 0.1 μF
C9 = (See Table II)

FIGURE 19 – Television IF Amplifier and Detector Using an MC1330 and an MC1352

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